A 0.8 V CMOS OTA and Its Application in Realizing a Neural Recording Amplifier

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***Abstract*—This work presents a low-voltage, low power CMOS symmetrical operational transconductance amplifier (OTA) and its application for realization of a biopotential amplifier in neural recording application. The linear range of OTA is increased by employing multi-tanh differential configuration and source degeneration while the common-mode range is enhanced using DC-shifting scheme. The proposed symmetrical OTA is operated with a single power supply of 0.8 V and shows an open loop gain of 31.6 dB with unit gain bandwidth of 202.3 KHz and using a 7 pF of load capacitor. A neural preamplifier was implemented in moderate inversion region using the proposed OTA. The preamplifier achieves 34.5 dB of gain consuming 77.1 μW of power and has an input referred noise of 24.18 μV_{rms} over 8.9 KHz of bandwidth.**

***Index Terms*—multi-tanh differential pair, low-voltage operational transconductance amplifier, neural preamplifier and moderate inversion**

I. Introduction

Recent times have seen some significant efforts to develop implantable electronic medical devices for biomedical applications. Some of which include devices like endoscopic capsule, artificial heart, artificial retinal prosthesis, and implantable ECG recorder. Traditionally, these devices are powered by implantable batteries which require low voltage supply for proper operation. However, with the limited energy budget of implantable batteries, the system performance becomes limited in terms of operating time, resolution, noise and so on.

Operational transconductance amplifier (OTA) is an important building block in integrated continuous-time filters. As the device sizes scale down, conventional saturation based OTAs face design challenges in terms of linearity and output impedance. OTA design techniques such as non-linearity cancelation [1] and adaptive biasing techniques [2] are commonly used to improve the linearity performance. However, it suffers from significant second-order harmonics partly from the saturation operation of MOSFETs and partly because of device mismatch due to process variation.

OTAs consisting of subthreshold differential pairs are attractive in biomedical applications because of their low power consumption, a low g_m transconductance and a high transconductance efficiency (g_m/I_D). Because of these features, it finds suitable use in efficient implementation in low frequency continuous time filters, for example from sub-10 Hz frequency range up to 10 KHz. Continuous-time linear filtering for applications such as bionic ears, is one class of analogue circuits for which subthreshold CMOS design is more challenging. Traditional differential pairs operating in weak inversion offer a linear range of few tens of mV. Several techniques for extending the linear range of differential pairs in weak inversion such as source degeneration via resistor/diodes, attenuation and nonlinear cancelation have been suggested in the literature [3]-[5].

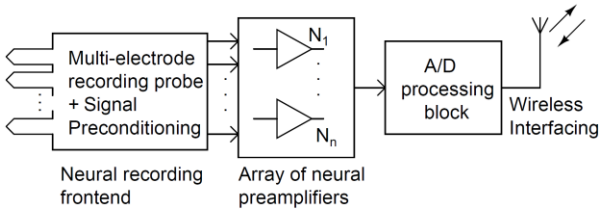

Figure 1. Analog front-end of implantable neural recording site.

The work reported here focusses on low voltage, low noise OTA design which can be used as a basic amplifier for invasive extracellular neural recording microdevices designed to record neural activities within the cerebral cortex. Fig. 1 illustrates the block diagram of an implantable neural recording microsystem comprising of several recording probes attached to a signal preconditioning module, a neural processing unit which is a part of analog preprocessing block, an A/D converter, and a wireless interfacing module. In this work we propose a very low voltage symmetrical OTA implemented with two differential pairs in parallel asymmetric multi-tanh configuration [6]. The proposed structure utilizes a DC shifting technique which exhibits linearity for a wide common-mode input range. Later on the OTA has been utilized to implement a neural recording preamplifier used in medical diagnostic method like electro-encephalography (EEG) and magnetic resonance imaging (MRI). The detailed noise analysis is also presented for both OTA as well as neural preamplifier followed by simulation performance and comparison with other similar biopotential amplifier designs.

II. Transconductor Design in Moderate Inversion

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A low voltage, low power operation of MOSFET is achievable by exploiting the subthreshold regime or weak inversion region. Nevertheless, designing CMOS circuits with devices in weak inversion have to compromise on the device shape factor resulting in large gate capacitance, low bandwidth, and high DC leakage [7], [8]. Moderate inversion offers a compromise of high (g_m/I_D) ratio, lower $V_{DS,sat}$ voltage and moderately high bandwidth necessary for power efficient, low voltage design. A relatively simple MOSFET model valid in all regions of operation: weak, moderate, and strong inversion is approximated from the EKV MOS model [9] by

$$I_D = I_S S\left[\ln\left(1+\exp\left\{\frac{\kappa\left(V_G - V_T\right)-V_S}{2U_T}\right\}\right)\right]^2 \quad (1)$$

UT = kT /q is the thermal voltage, S=W/L the width to length ratio, κ (= 1/n) is the gate coupling coefficient and represents the coupling of the gate to the surface potential. *n* is the constant parameter depending on the technology (typically 1.5 near weak inversion), while IS is the subthreshold current-scaling parameter strongly dependent on the temperature.

$$I_S = 2n\mu C_{ox}U_T^2 \quad (2)$$

Cox is the gate-oxide capacitance per unit area, μ is channel carrier mobility. The MOS transistor biased at weak side of moderate inversion must comply with the following requirement: -72 mV < $V_{EFF}(= V_{GS} - V_T)$ < 40 mV, $V_{DS} > 3U_T$ for weak saturation while I_D can be evaluated from the condition $I_D < 2nK_n' \frac{W}{L}U_T^2$, where $K_n' = \mu_n C_{ox}$ is a transconductance parameter of an n-channel MOS transistor.

III. Proposed Scheme

Fig. 3 shows the basic schematic of the proposed OTA operated in subthreshold. The proposed OTA consists of transconductor with two asymmetric differential pairs implemented by transistors M_{1a}-M_{1b} and M_{2a}-M_{2b} connected in parallel. The effect of unequal sizing of the transistor pairs is to create an intentional voltage offset. To further increase the input linear range, single diffusor is used as a means of source degeneration with each differential pair. The conductivity of the diffusor is determined by the respective *W/L* ratio and the applied gate potential, V_C. The proposed circuit is thus a large-signal transconductor, where transconductance g_m can be tuned through the control voltage V_C . The differential current I_0 can be obtained in terms of differential input voltage, $V_{dm} = V_{in+} - V_{in-}$ as

$$I_0 = I_{BIAS}\tanh\left(\frac{V_{dm}}{2nU_T}+\frac{1}{2}\ln m\right)+I_{BIAS}\tanh\left(\frac{V_{dm}}{2nU_T}-\frac{1}{2}\ln m\right) \quad (3)$$

where m is the relative *W/L* ratio of the transistor pairs. A possible criteria for optimizing the linear range is maximal flatness [1]. Approximating $m = 4$ introduces equal and opposite input differential voltage offset resulting in maximum nonlinearity cancelation in transistor pairs $M_{1a,b}$ and $M_{2a,b}$.

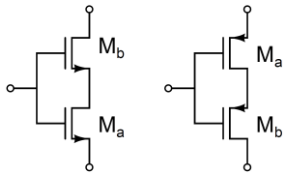

Figure 2. n-type and p-type composite transistors with common well.

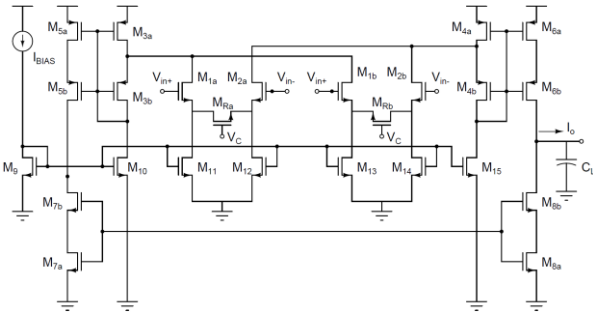

Figure 3. Subthreshold OTA with symmetric multi-stage balanced operation

A composite transistor formed with two series connected n-type or p-type MOS transistor having the same well is an important configuration for subthreshold circuits [10] as depicted in Fig. 2. Noting that $V_{DSa} = V_{GSa} - V_{GSb}$, equating the drain currents, I_{DSa} and I_{DSb} with voltage V_{DSa} applied so that M_b is in weak saturation, we obtain the following relationship:

$$V_{DSa} = U_T \ln\left[1+\frac{(W/L)_b}{(W/L)_a}\right] \quad (4)$$

Note that the drain-source voltage of saturate transistor is independent of gate-source voltage. Moreover V_{DSa} is not effected by a changing V_{DSb} .

The composite transistor structure is implemented in Fig. 3 where pMOS device pairs M_{3a} - M_{3b} , M_{5a} - M_{5b} and M_{4a} - M_{4b} , M_{6a} - M_{6b} form a composite transistors while transistors M_{3b} and M_{4b} function as level shifters. This forces drain voltage of differential pairs to be equal since drain voltages of M_{3a} and M_{4a} are equal and constant thus ensuring an optimal match for each of differential stages M_{1a} - M_{2a} and M_{1b} - M_{2b} . As the active load and the differential amplifiers are biased at the same potential therefore the voltage V_{DS3a} can be expressed as

$$V_{DS3a} = U_T \ln\left[1+2\frac{(W/L)_{3b}}{(W/L)_{3a}}\right] \quad (5)$$

An analogous expression can also be obtained for V_{DS4a}.

The expression for the third order harmonic distortion for the input transistors can be derived by expanding equation (3) through Taylor series:

$$I_0 = \frac{8m}{(m+1)^2}\left[\frac{V_{dm}}{2nU_T} - \left(\frac{4m}{(m+1)^2}-\frac{2}{3}\right)\left(\frac{V_{dm}}{2nU_T}\right)^3\right] \quad (6)$$

From above equation HD_3 can be defined as the ratio between coefficients of third order harmonic and the fundamental.

$$HD_3 = \frac{1}{4}\left|\frac{4m}{(m+1)^2}-\frac{2}{3}\right|\left(\frac{V_{dm}}{2nU_T}\right)^2 \quad (7)$$

By choosing $m=4$, the maximum input differential signal can be computed for a given HD_3 specification. Thus the multi-tanh scheme gives better improvement in linearity as compared to a conventional differential amplifier design.

A. AC Model

The AC model of the proposed OTA is represented with equivalent small signal model of all elements along signal path. By taking advantage of the symmetry, the proposed OTA of Fig. 3 can be replaced with the π equivalent model as shown in Fig. 4. Here input tranconductance is given by $g_{m2} = g_{m2a} + g_{m2b}$ while the output resistance due to channel length modulation is $r_{o2} = 1/g_{o2} = (r_{o2a} \| r_{o2b})$. The parasitic capacitance C_1 is due to the drain node of the rail transistor M_{6a} while C_L is the load capacitor. The DC gain can be obtain by ignoring all capacitances in the circuit.

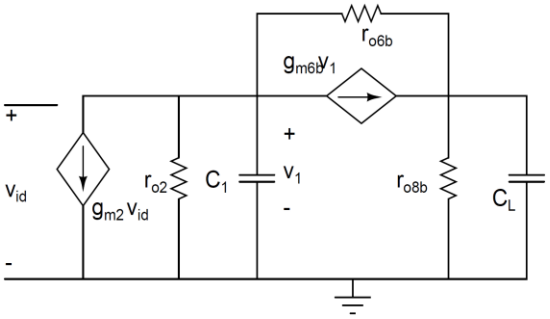

Figure 4. Small signal model of symmetric OTA.

$$A_{v,dc} = \frac{g_{m2}}{g_{o2}\left(\frac{g_{o6b}+g_{o8b}}{g_{m6b}+g_{o6b}}\right)+g_{o8b}} \quad (8)$$

The OTA's dominant pole frequency is found to be

$$\omega_d = \frac{g_{m2}}{A_{v,dc}C_L\left(1+\frac{g_{o2}}{g_{m6b}+g_{o6b}}\right)} \quad (9)$$

The parasitic capacitances due to the increased number of nodes caused by level shifter arrangement do not deter OTA's dominant pole location and is still decided by the load capacitor C_L. As $g_{o2} \ll (g_{m6b}+g_{o6b})$, the dominant pole frequency can be approximated to $f_d = g_{m2}/2\pi A_{v,dc}C_L$.

B. Noise Analysis of OTA

$$\overline{V_{OTA,th}^2} = 2(4kT)\left[\frac{2(n\Gamma)_1 g_{m1}}{G_M^2}+\frac{(n\Gamma)_3 g_{m3}}{G_M^2}+\frac{(n\Gamma)_5 g_{m5}}{G_M^2}+\frac{(n\Gamma)_7 g_{m7}}{G_M^2}+\frac{(n\Gamma)_{10} g_{m10}}{G_M^2}\right] \quad (10)$$

$$\overline{V_{OTA,f}^2} = \frac{2}{C_{ox}}\frac{1}{f}\left[\frac{2K_{f1}g_{m1}^2}{(WL)_1 G_M^2}+\frac{K_{f3}g_{m3}^2}{(WL)_3 G_M^2}+\frac{K_{f5}g_{m5}^2}{(WL)_5 G_M^2}+\frac{K_{f7}g_{m7}^2}{(WL)_7 G_M^2}+\frac{K_{f10}g_{m10}^2}{(WL)_{10} G_M^2}\right] \quad (11)$$

The input gate-referred thermal noise voltage density is mainly dominated by the self-cascode current mirror devices $M_{7,8}$ and the current drivers $M_{10,15}$ since one or more of these transistors are operating in strong inversion for the same drain current flowing through these devices. The input transistor pair, $M_{1,2}$ and the composite transistor pairs M_{3-6} which lie along the signal path also contribute to thermal noise. Noise from the tail current sources M_{11-14} and its external reference device is canceled-out since they are largely common-moded. The OTA input-referred thermal noise voltage, power spectral density (PSD) is given by equation (10). Here kT is the product of Boltzmann's constant and absolute temperature. $(n\Gamma)_1$, $(n\Gamma)_3$, $(n\Gamma)_5$, $(n\Gamma)_7$, and $(n\Gamma)_{10}$ are the products of the substrate factor, n, and thermal noise factor Γ for respective devices where Γ is expressed as

$$\Gamma = \frac{\frac{1}{2}+\frac{2}{3}IC}{1+IC} \quad (12)$$

Γ is expressed in terms of inversion coefficient factor IC of the EKV model [11], given by

$$IC = \frac{I_D}{2n\mu C_{ox}U_T^2(W/L)} = \frac{I_D}{I_S(W/L)} \quad (13)$$

with symbols having their usual meaning. To obtain the noise level the input referred thermal noise density can be integrated over the bandwidth $\Delta f = f_2 - f_1$. Equation (10) integrated in the desired band of frequency, namely f_1 to f_2 gives

$$\overline{V_{OTA,t,th}^2} = \int_{f_1}^{f_2} \overline{V_{OTA,th}^2} df = \frac{8KT\Delta f}{G_M^2} \sum_i (n\Gamma)_i \, g_{mi} \quad (14)$$

where i =1,2,3,5,7,10. The input referred flicker noise voltage PSD for the OTA is given by equation (11).

In the given equation K_{fi} is the flicker noise factor and is a process-dependent parameter, f is the operating frequency, and G_M is the output transconductance of the OTA given as:

$$G_M = \frac{g_{m2}\left(g_{m6b} + g_{o6b}\right)}{g_{m6b} + g_{o6b} + g_{o2}} \approx g_{m2} \quad (15)$$

Integrating flicker noise density over the desired bandwidth gives

$$\overline{V_{OTA,t,f}^2} = \int_{f_1}^{f_2} \overline{V_{OTA,f}^2} df = \frac{2}{C_{ox} G_M^2} \ln\left(\frac{f_2}{f_1}\right) \sum_i \frac{K_{fi} g_{mi}^2}{(WL)_i} \quad (16)$$

The total input referred noise of the OTA consisting of both thermal and flicker noise power spectral density integrated over the bandwidth defined by $\Delta f = f_2 - f_1$ can be computed as

$$\overline{V_{n,OTA}^2} = \sum_i \left[\frac{8KT\Delta f}{G_M^2} (n\Gamma)_i \, g_{mi} + \frac{2\ln(f_2 / f_1)}{C_{ox} G_M^2} \frac{K_{fi} g_{mi}^2}{(WL)_i} \right] \quad (17)$$

C. Common Mode Feedback for the OTA

A common-mode feedback (CMFB) circuit is an indispensable part of a fully differential OTA. A CMFB circuit should ideally be designed to have a very small impedance for the common-mode signals but transparent for the differential signals. Taking care of this feature helps in reducing harmonic distortion components and improve THD and HD_3 response of the circuit. Since the proposed OTA is not intended for very large voltage swing therefore the common-mode feedback is implemented by differential-difference amplifier structure [12] which uses four identical transistors to average and compare the common-mode voltages. The transconductance gain of CMFB as shown in Fig. 5 is kept optimally higher in order to minimize the common-mode noise voltage of OTA. Nevertheless, transconductance gain can be reduced for input transistors $M_{16a,b,c,d}$ thereby reducing (W/L) ratios of the MOS transistors and by increasing the bias current source, I_b thus securing linearity to some extent. The difference between the common mode voltage and V_{ref} is amplified by the error amplifier M_{18} and output current is fed back to the gate of OTA source transistors. The non-dominant poles caused due to the internal nodes of CMFB appear at much higher frequencies than the dominant pole at f_d and can be neglected.

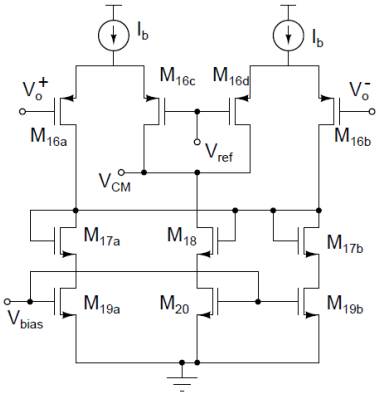

Figure 5. Common mode feedback employed for symmetric OTA.

D. Design of the Proposed Transconductor

The overall circuit of CMFB-OTA gives a core current consumption of 96.4 μ A, with input device drain currents of 7 μ A and power consumption of 77.1 μ W which excludes bias reference current and voltage sources. The symmetrical OTA output stage is implemented with $M_{7a,b}$ and $M_{8a,b}$ self-cascoded structure which are meant to increase the output resistance without having extra voltage headroom. Here the aspect ratios of M_{7b} and M_{8b} cascode devices are kept much larger than that of M_{7a} and M_{8a} rail devices for obtaining high output impedance without sacrificing common-mode linear range operation suitable for low voltage application. As seen from equation (15), G_M is nearly equal to the transconductance of the input pair devices because current mirrors consisting of self-cascode structures route signal currents from the input pair drains to the OTA output with nearly unity current gain. Evaluating output resistance of the OTA gives:

$$R_{out} = \frac{g_{m6b} + g_{o6b} + g_{o2}}{g_{m6b} g_{o8b} + g_{o2} g_{o6b} + g_{o8b} g_{o2} + g_{o6b} g_{o8b}} \quad (18)$$

It is clear from the voltage gain, $A_{v,dc}$, which is product of the G_M from equation (15) and R_{out} from equation (18) that $A_{v,dc}$ of the proposed OTA can be maximized by operating input pair devices at low inversion coefficients when biased more towards weak inversion region for high $g_{m1,2} / I_{D1,2}$ and $g_{m1,2}$, also combined with operating output devices M_{5-8} at long channel length for obtaining lower output conductance.

IV. A Neural Amplifier Using Proposed Transconductor

A. Design of Neural Amplifier

To measure the validity and feasibility of the proposed OTA topology, a preamplifier using our OTA was designed for neural prosthetic application. Neural signal

from extra-cellular recording are very weak in amplitude (varying from 10 μ V to 500 μ V). As a result amplification is needed before they can be further processed. A neural amplifier is typically implemented either as a double-ended (DCCA) [13] or as a single-ended capacitively coupled (SCCA) preamplifier [14]. We have used the latter approach for our preamplifier design as depicted in Fig. 6. It consists of a closed-loop gain along with a low-frequency pole using a capacitive feedback network and a MOS-bipolar pseudo resistor which is made highly resistive through proper gate voltage biasing. The lower 3-dB cut-off frequency of bandwidth is given by

$$\omega_L = 2\pi f_L = \frac{1}{\mathrm{R}_{eq} C_f} \tag{19}$$

where C_f is the capacitor in feedback loop and R_{eq} is the equivalent resistance of series connected bipolar-MOS elements. Thus ω_L can be tuned using this gate voltage V_{tune} to control the impedance in the feedback and enabling selection or rejection of slow wave action potentials. The upper cut-off frequency is governed by the dominant pole frequency ω_U .

$$\omega_U = \frac{G_M}{A_v C_L} \tag{20}$$

The mid-band gain A_v appearing in equation (20) is approximated by the ratio of input capacitance to the capacitance in negative feedback.

$$A_v = \left|\frac{v_0}{v_{in}}\right| = \frac{C_i / C_f}{1 + \frac{1}{A_{v,dc}}\left(1 + \frac{C_i}{C_f}\right)} \approx \frac{C_i}{C_f} \tag{21}$$

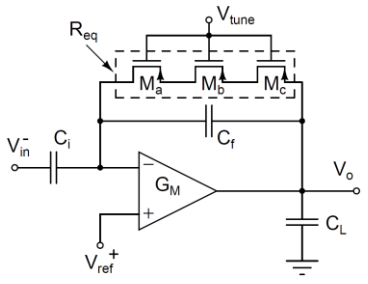

Figure 6. Schematic of a neural preamplifier.

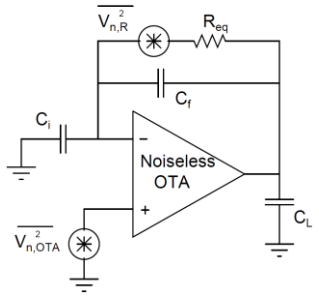

Figure 7. Noise model of the neural preamplifier.

B. Noise Analysis of Neural Amplifier

The noise of the resulting neural amplifier of Fig. 6 can be evaluated using the equivalent noise model as shown in Fig. 7.

The noise power density of the pseudo-resistor having equivalent resistance of R_{eq} is represented by $\overline{V_{n,R}^2} = 4kTR_{eq}$ as the thermal noise. The input referred noise of the proposed OTA $V_{n,OTA}^2$ as given by equation (17), is placed as a noise source at the input of the noiseless OTA. The noise spectrum of the resistor $\overline{V_{in,R}^2(f)}$ is shaped by low-pass characteristics:

$$\overline{V_{in,R}^2(f)} = \frac{\overline{V_{n,R}^2}}{A_v^2\left[1+\left(2\pi f R_{eq} C_f\right)^2\right]} \approx \overline{V_{n,R}^2}\left(\frac{f_L}{A_v f}\right)^2 \tag{22}$$

The input noise spectral density of the OTA is calculated as

$$\overline{V_{in,OTA}^2(f)} = \frac{\overline{V_{n,OTA}^2}}{A_v^2}\left[\left(1+\frac{C_i}{C_f}\right)^2 + \left(\frac{1}{2\pi f R_{eq} C_f}\right)^2\right] \tag{23}$$

The pseudo-resistor has thermal noise PSD $\overline{V_{in,R}^2(f)}$ with power characteristics of brown noise ($1/f^2$) while the OTA noise is increased due to capacitive transformation. The second term in equation (23) can be ignored since spectrum of $\overline{V_{in,OTA}^2(f)}$ is only significant at much lower frequencies ($f \ll (f_L / A_v)$) than the band of interest.

V. Simulation Results and Discussion

A. Simulation Results of CMFB-OTA

The proposed symmetrical OTA of Fig. 6 terminated with a 7 pF of load capacitor was simulated in Cadence Spectre of standard UMC 0.18 μ m CMOS process technology operated at $27^{\circ}C$. The threshold voltages of nMOS and pMOS transistors are 315 mV and 498 mV respectively. The OTA design considers multi-tanh input transistor pairs $M_{1a,2a}$ and $M_{1b,2b}$ to be perfectly matched and working towards the weaker edge of moderate inversion region. Large transistor dimensions are maintained at the input (in multiple of $10\mu m/10\mu m$) to ensure minimal flicker noise pushing flicker noise corner frequency to sub-hertz range. The OTA-CMFB circuit draws 96.38 μ A of current operating with a single supply of $+0.8$V.

As was predicted earlier, the linear input range extension by using DC shifting and current cancelation technique, the measured input linear range as shown in Fig. 9 is 157 mV for $HD_3 \le 1\%$ which is sufficient for

neural recording application and can be suited to many other biomedical applications [15], [16]. The maximum signal swing was observed from 0 to 500 mV while the measured transconductance gain was 17.85 μ A/V. The G_M value is relatively high because of the increased $I_{D1,2}$ since it is the product of g_m / I_D and I_D where g_m / I_D ratio for input devices is chosen high owing to the operation near weak inversion region.

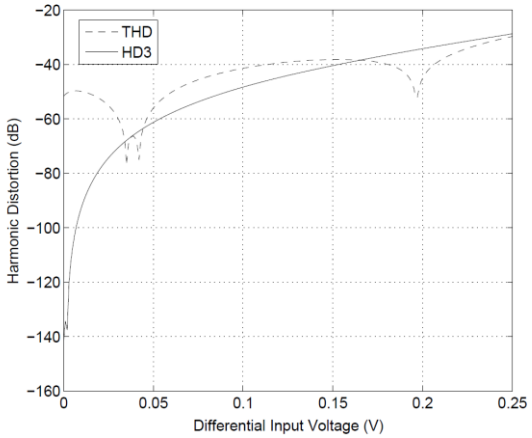

Figure 8. THD and HD3 simulation of symmetric OTA.

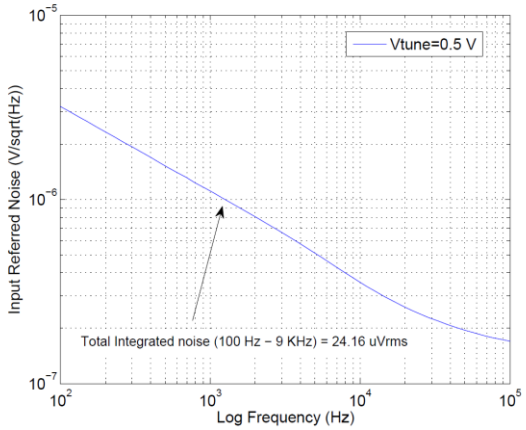

Figure 9. Input-referred noise density simulation by Cadence Spectre.

g_m / I_D can be generalized in terms of inversion coefficient IC which is valid for all region of operation and is given by

$$\frac{g_m}{I_D} = \frac{1}{nU_T\left(\sqrt{IC+0.25}+0.5\right)} \quad (24)$$

The operating region can be defined with respect to the inversion coefficient; the device operating in weak inversion will have $IC < 0.1$, for device operating in moderate inversion, $0.1 < IC < 10$, while for the devices operating in strong inversion, $IC > 10$. Table I shows device dimensions and operating point of MOS devices in the proposed OTA circuit. The frequency response of OTA-CMFB structure showed the open loop DC gain as 31.6 dB and a unit gain bandwidth of 202.3 KHz with 90.18° of phase margin.

TABLE I. OPERATING POINT OF DEVICES IN OTA

Devices	W/L (μm)	gm/ID (V^{-1})	IC
$M1a,2a$	10/10	23.83	0.40
$M1b,2b$	40/10	23.77	0.40
$M3a,4a,5a,6$	700/0.8	18.72	1.10
$M3b,4b,5b,6$	160/0.8	24.25	0.36
$M7a,8a$	20/2	15.07	2.20
$M7b,8b$	160/2	23.09	0.47
$M10,15$	10/2	11.94	4.19

B. Simulation Results of Neural Amplifier

Simulation results of the input referred noise power spectral density is shown in Fig. 9. With the positive gate voltage of V_{tune} = 0.5 V applied to transistors $M_{a,b,c}$ the parasitic BJT behavior sets in the lateral path along source, well and drain giving high incremental resistance of the order of peta-ohms. The noise calculation was done by using flicker noise parameters from the parameter extraction of nMOS and pMOS transistors using BSIM3v3 model and were evaluated as $K_f = 1.06\times10^{-25}$ V ^{2} F for nMOS and $K_f = 9.07\times10^{-27}$ V ^{2} F for pMOS. The integrated input referred noise was found to be 24.16 $\mu V / \sqrt{Hz}$ over (0.1 - 9.0) KHz bandwidth.

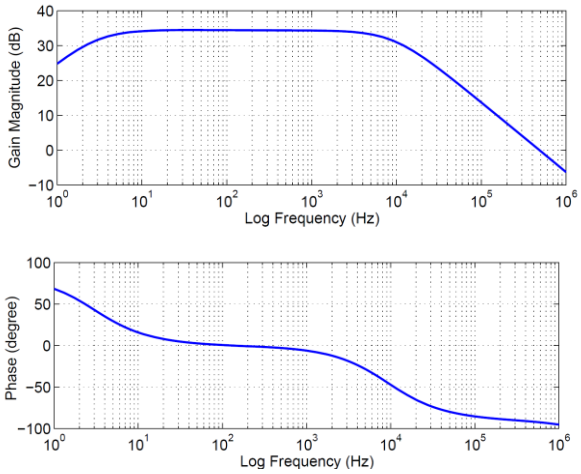

Figure 10. Gain and phase plot of the neural preamplifier.

Simulation results of the frequency response of the preamplifier transfer function are shown in Fig. 10. With the input capacitor C_i = 6 pF and the capacitor in feedback C_f = 100 fF, the mid band gain was found to be 34.5 dB over a bandwidth of 2.9 Hz to 9.2 KHz. The lower 3-dB frequency can be tuned via V_{tune} voltage by varying the effective channel conductance in the feedback loop. The total harmonic distortion (THD) was remained below 1 % for differential input less than 9.11

mV. The common mode rejection as shown in Fig. 11 was measured and was found to be better than 43 dB.

TABLE II. SUMMARY OF PERFORMANCE AND COMPARISON WITH NEURAL PREAMPLIFIERS DESIGNED IN CMOS

Parameter	[17]	[18]	[13]	[19]	[20]	This work
CMOS Technology	1.5 μm	0.35 μm	1.5 μm	1.5 μm	0.35 μm	0.18 μm
Supply Voltage	1.5V	3.0V	±2.5V	1.5V	3.0V	0.8V
DC Gain	42.5dB	38.1dB	39.5dB	39.3dB	33dB	34.5dB
Operating frequency	22Hz-6.7KHz	1.4Hz-8.5KHz	25mHz-7.2KHz	DC-9.1KHz	0.5Hz-10KHz	3Hz-9.2KHz
Input referred Noise	20.6 $\mu Vrms$	14.4 $\mu Vrms$	2.2 $\mu Vrms$	7.8 $\mu Vrms$	6.08 $\mu Vrms$	24.16 $\mu Vrms$
Noise BW	10Hz-10KHz	1.4Hz- 8.5KHz	0.025Hz-7.2KHz	0.1Hz- 10KHz	10Hz- 5KHz	100Hz-9KHz
THD	–	1%@2.4mV_{pp}	1%@12.4mV_{pp}	–	1.1%@5mV_{pp}	1%@9.1mV_{pp}
Power Consumption	0.8 μW	6 μW	80 μW	115 μW	8.4 μW	77.1 μW

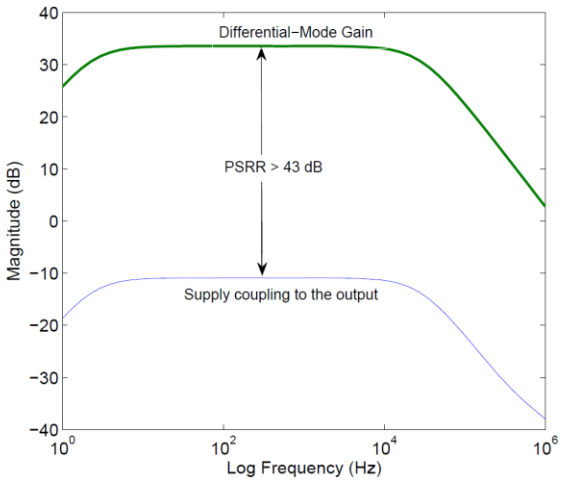

Figure 11. PSRR response of the neural preamplifier.

The comparative performance of neural recording amplifiers based on fully-integrated design is shown in Table II. The amplifiers taken for comparison in Table II were designed in CMOS with the power consumption per channel in the range of microwatts with no off-chip components. The CMOS design in this work provides the lowest power supply design having comparable power level and the overall gain with very low distortion components.

VI. CONCLUSION

A 0.8 V CMOS biosignal amplifier used in neural recording application was successfully designed and simulated. The single-ended capacitively-coupled neural preamplifier gave an input-referred noise of 24.16 μV while consuming 77.1 μW of power and having flat-band gain of 34.5 dB over a frequency range of 2.9 Hz to 9.2 KHz. The noise performance could further be improved by using pMOS devices as input differential pair and reducing flicker noise current associated with non-input devices. By maintaining proper g_m / I_D ratios, input MOS devices in the proposed design are operated at the edge of weak and moderate inversion region and non-input devices towards strong inversion region so as to achieve maximum power efficiency and an optimal flicker noise voltage PSD while operating on a limited power supply. A fully differential OTA with common-mode feedback was designed as a basic amplifier for neural pre-amplification. Current cancelation, source degeneration, and DC-shifting techniques were used for linearity improvement of the OTA while self cascode structure was employed at the output stage to further enhance the DC gain. The proposed OTA can suitably be used in low voltage, low frequency, and low THD biomedical OTA-C filter applications.

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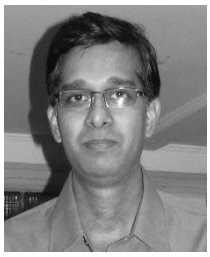

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